IN THE CLAIMS

1. (Previously Presented) A method of fabricating a source interconnect to a memory cell, comprising:

forming a layer of dielectric material overlying a gate stack, a source region and a drain region of the memory cell;

forming a first mask layer overlying the layer of dielectric material;

patterning the first mask layer to expose a portion of the layer of dielectric material over at least the source region;

removing a portion of the exposed portion of the layer of dielectric material to form a trench shaped region and expose the source region;

removing the first mask layer;

forming a layer of polysilicon overlying the layer of dielectric material and trench shaped region to be in contact with the exposed source region;

forming a second mask layer overlying the layer of polysilicon;

patterning the second mask layer to expose a portion of the layer of polysilicon over at least the trench shaped region;

implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon;

removing the second mask layer; and

selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region.

2. (Currently Amended) The method of claim 1, wherein forming a first and ~~and/or~~ second mask layer further comprises forming ~~a~~ at least one of the first and ~~and/or~~ second mask layer with a photoresist.

3. (Previously Presented) The method of claim 1, wherein patterning the first and second mask layers further comprises patterning the first and second mask layers with the same pattern.

4. (Previoulsy Presented) The method of claim 1, wherein forming a layer of polysilicon overlying the layer of dielectric material and trench shaped region to be in contact with the exposed source region further comprises forming a layer of polysilicon overlying the layer of dielectric material and trench shaped region to be in contact with the exposed source region, wherein the layer of polysilicon is conductively doped.

5. (Original) The method of claim 1, wherein selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect further comprises selectively wet etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect.

6. (Original) The method of claim 5, wherein wet etching further comprises wet etching with TMAH.

7. (Cancelled)

8. (Previously Presented) The method of claim 5, wherein wet etching further comprises wet etching with KOH.

9. (Original) The method of claim 1, wherein forming a layer of polysilicon overlying the layer of dielectric material and in contact with the exposed source region further comprises forming a layer of silicon-containing material overlying the layer of dielectric material and in contact with the exposed source region.

10. (Original) The method of claim 1, wherein patterning first mask layer further comprises patterning first mask layer to expose a portion of the layer of dielectric over the source region and a portion of the gate stack.

11. (Original) The method of claim 1, wherein patterning second mask layer further comprises patterning second mask layer to expose a portion of the layer of polysilicon over the source region and a portion of the gate stack.

12. (Original) The method of claim 1, wherein implanting ions further comprises implanting ions with a dosage level in the range of $1x10^{15}$ ions per cm^3 to $1x10^{22}$ ions per cm^3.

13. (Original) The method of claim 12, wherein the ion dosage level is in the range of $5x10^{18}$ ions per cm^3 to $5x10^{20}$ ions per cm^3.

14. (Original) The method of claim 1, wherein implanting ions further comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon, and silicon.

15. (Currently Amended) The method of claim 1, wherein removing the first and ~~and/or~~ second mask layer further comprises stripping at least one of the first and ~~and/or~~ second mask layer.

16. (Original) The method of claim 1, wherein removing a portion of the exposed portion of the layer of dielectric material to expose the source region further comprises anisotropically etching the exposed portion of the layer of dielectric material.

17. (Previously Presented) The method of claim 1, wherein patterning the first and second mask layers further comprises patterning the first mask layer to additionally expose a portion of the layer of dielectric over the drain region and patterning the second mask layer to expose a portion of the layer of polysilicon over the drain region.

18 – 87. (Canceled).